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10/560,687	12/14/2005	Francesco Pessolano	NL 030671	1945

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EXAMINER	
HUYNH, PHUONG	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,687	PESSOLANO ET AL.	
	Examiner	Art Unit	
	PHUONG HUYNH	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-2, 10-20 and 27-29** are rejected under 35 U.S.C. 102(b) as being anticipated by Buer et al. (hereinafter "Buer") (USPN. 6,114,880).

Regarding claim 1, Buer discloses an integrated circuit comprising a timing closure monitoring circuit for monitoring timing closure in a logic path on the integrated circuit, the logic path being clocked by a clock signal, and the timing closure monitoring circuit comprising:

a signal generator [14] for generating a predetermined reference signal [see Buer: col. 2, lines 53-65; col. 3, lines 23-28]; a duplicate logic path [20] having characteristics matched with the logic path being monitored [see Buer: col. 3, lines 44-50], and connected to receive the reference signal from the signal generator [see Buer: col. 2, lines 53-65; col. 3, 17-27]; and monitoring circuit [28] arranged to receive an output signal from the duplicate logic path, to compare receipt of the output signal relative to receipt of the clock signal, and to provide

an output signal indicative of the status of the timing closure in the logic path being monitored [see Buer: col. 3, lines 8-27; and col. 4, lines 10-30].

Regarding claim 2, Buer discloses that the timing closure signal indicates a timing violation when the output signal of the duplicate logic path is delayed by a predetermined amount [see Buer: col. 4, lines 18-30].

Regarding claim 10, Buer discloses that the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored [see Buer: col. 3, lines 44-51].

Regarding claim 11, Buer discloses that the duplicate logic path includes one or more buffer stages for matching the characteristics of the logic path being monitored [see Buer: col. 4 lines 9-17].

Regarding claim 12, Buer discloses that the one or more buffer stages comprise the same number of switching gates as the logic path being monitored [see Buer: col. 4, lines 3-9].

Regarding claim 13, Buer discloses that the timing closure violation signal is used to generate an interrupt signal [see Buer: col. 4, lines 10-28].

Regarding claim 14, Buer discloses that the timing closure violation signal [freq error] is supplied to a second timing closure monitoring circuit [30] on the integrated circuit, the first and second timing closure monitoring circuits generating a serial interrupt signal [see Buer: col. 4, lines 3-58].

Regarding claim 15, Buer discloses that the logic path being monitored is a critical path in the integrated circuit [see Buer: col. 2, lines 53-60].

Regarding claim 16, Buer discloses one or more further timing closure monitoring circuits, for monitoring timing closure in one or more further logic paths on the integrated circuit [see Buer: col. 2, lines 53-65; col. 3, lines 23-28; and col. 4, lines 10-30]. Although Buer does not explicitly disclose “one or more further monitoring circuits”, Buer still discloses the claimed “one or more monitoring circuits” because these are duplicate part for multiple effects and this generally does not provide patentable weight to the claimed invention. See St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977).

Regarding claim 17, Buer discloses that the monitoring circuit includes a latch [see Buer: col. 3, lines 10-28; and lines 51-63].

Regarding claim 18, Buer discloses that the output signal of the monitoring means is used to control the timing closure in the logic path being monitored [see Buer: col. 4, lines 10-28; and lines 37-57].

Regarding claim 19, Buer discloses a method of monitoring timing closure in a logic path on an integrated circuit, the method comprising:

generating a predetermined reference signal [see Buer: col. 2, lines 53-65; col. 3, lines 23-28]; providing a duplicate logic path [20] corresponding to the logic path being monitored, the logic path being clocked by a clock signal [CLK] [see Buer: col. 2, lines 53-65]; passing the reference signal through the duplicate logic path [see Buer: col. 3, lines 17-37], and monitoring receipt of the output of the duplicate logic path relative to receipt of the clock signal [CLK], and using the output of the duplicate logic path to produce a timing closure signal indicative of the status of the timing closure in the logic path being monitored based on the monitoring of the receipt of the output of the duplicate logic path relative to the receipt of the clock signal [see Buer: col. 3, lines 45-57; and col. 4, lines 10-30].

Regarding claim 20, Buer discloses that the output signal indicates timing closure violation when the output of the duplicate path is delayed by a predetermined amount [see Buer: col. 4, lines 18-30].

Regarding claim 27, Buer discloses that the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored [see Buer: col. 3, lines 44-51].

Regarding claim 28, Buer discloses that the logic path being monitored is a critical path in the integrated circuit [see Buer: col. 2, lines 53-60].

Regarding claim 29, Buer that the duplicate logic path is initially determined by: identifying a critical logic path in the integrated circuit [see Buer: col. 2, lines 53-65; col. 3, lines 23-28]; decomposing the critical path into one or more stages [see Buer: col. 2, line 65-col. 3, line 28]; constructing buffer stages [22, 22A, 22B] corresponding to the stages identified in the decomposing step [see Buer: col. 3, line 45-51; col. 3, line 64-col. 4, line 15], the buffer stages being constructed to have the *same characteristics* as the stages of the critical path being monitored [see Buer: col. 4, lines 1-15]; and composing the duplicate path using the buffer stages constructed in the constructing step [see Buer: col. 4, lines 10-30].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 3-6, 8-9, 21-23, 25 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Buer et al. (hereinafter “Buer”) (USPN. 6,114,880) in view of Chuang et al. (hereinafter "Chuang") (US Patent App. Pub. No. 2003/0128606).

Regarding claim 3, Buer discloses that the clock signal [CLK] is used by the signal generator to generate the reference signal [see Buer: col. 3, lines 8-27], and wherein the timing closure signal indicates a timing closure violation when the output signal of the duplicate logic path is received by the morning circuit; [see Buer: col. 4, lines 31-57]; but not “after the monitoring circuit receives a next leading edge of the clock signal”.

Chuang teaches wherein the timing closure signal indicates a timing closure violation when the output signal of the duplicate logic path is received by the morning circuit after the monitoring circuit receives a next leading edge of the clock signal [see Chuang: Paragraphs [0040] and [0046]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant’s invention to modify the invention of Buer to include the method, as taught by Chuang, to provide an unchanged select signal pulse width [see Chuang: Paragraphs [0040] and [0046]].

Regarding claim 4, Buer and Chuang discloses everything as applied above [see claims 1 and 3]. In addition, Buer discloses that the reference signal

produced by the signal generator is synchronized with the clock signal [see Buer: col. 3, lines 8-27].

Regarding claim 5, Buer does not disclose that the reference signal is synchronized with the leading edge of the clock signal.
Chuang teaches that the reference signal is synchronized with the leading edge of the clock signal [see Chuang: Paragraphs [0040] and [0046]].
It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the signal, as taught by Chuang, to provide an unchanged select signal pulse width [see Chuang: Paragraphs [0040] and [0046]].

Regarding claim 6, Buer discloses that the reference signal produced by the signal generator is delayed with respect to the clock signal [see Buer: col. 3, lines 45-57].

Regarding claim 8, Buer does not disclose that the signal generator is configured to generate a reference signal having a pulse width that is predetermined according to a design margin.
Chuang teaches that the signal generator is configured to generate a reference signal having a pulse width that is predetermined according to a design margin [see Chuang: Paragraphs [0032] and [0036]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the signal, as taught by Chuang, to improve overall performance, and enhance circuit robustness [see Chuang: Paragraphs [0032] and [0036]].

Regarding claim 9, Buer does not disclose that the design margin determines the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.

Chuang teaches that the design margin determines the sensitivity of the timing closure monitoring circuit for detecting timing closure violation [see Chuang: Paragraphs [0032] and [0036]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the design margin, as taught by Chuang, to improve overall performance, and enhance circuit robustness [see Chuang: Paragraphs [0032] and [0036]].

Regarding claim 21, Buer discloses that the clock signal [CLK] is used to generate the reference signal [see Buer: col. 3, lines 8-27] and wherein the timing closure signal indicates a timing closure violation [see Buer: col. 4, lines 31-57] but not "when a next leading edge of the clock signal precedes the output of the duplicate logic path".

Chuang teaches wherein the timing closure signal indicates a timing closure violation when a next leading edge of the clock signal precedes the output of the duplicate logic path [see Chuang: Paragraphs [0040] and [0046]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the method, as taught by Chuang, to provide an unchanged select signal pulse width [see Chuang: Paragraphs [0040] and [0046]].

Regarding claim 22, Buer and Chuang discloses everything as applied above [see claims 19 and 21 above]. In addition, Buer discloses that the reference signal is synchronized with the clock signal [see Buer: col. 3, lines 8-27].

Regarding claim 23, Buer and Chuang discloses everything as applied above [see claims 19 and 21 above]. In addition, Buer discloses that the reference signal is delayed with respect to the clock signal [see Buer: col. 3, lines 45-57].

Regarding claim 25, Buer does not disclose that the pulse width of the reference signal is chosen according to a predetermined design margin.

Chuang teaches that the pulse width of the reference signal is chosen according to a predetermined design margin [see Chuang: Paragraphs [0032] and [0036]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include pulse width, as taught by Chuang, to improve overall performance, and enhance circuit robustness [see Chuang: Paragraphs [0032] and [0036]].

Regarding claim 26, Buer does not disclose that the design margin relates to the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.

Chuang teaches the design margin relates to the sensitivity of the timing closure monitoring circuit for detecting timing closure violation [see Chuang: Paragraphs [0032] and [0036]].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the design margin, as taught by Chuang, to improve overall performance, and enhance circuit robustness [see Chuang: Paragraphs [0032] and [0036]].

5. **Claims 7 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Buer et al. (hereinafter "Buer") (USPN. 6,114,880) and Chuang et al. (hereinafter

"Chuang") (US Patent App. Pub. No. 2003/0128606) as applied to claims 6 and 23; and further in view of Flautner et al. (hereinafter "Flautner") (USPN. 7,278,080).

Regarding claims 7 and 24, Buer disclose wherein the reference signal is delayed with respect to the clock signal [see Buer: col. 3, lines 8-27], *but not* by an amount equal to (prop_delay) - (1/2 design_margin), where (prop_delay) is the propagation delay of a processing unit driving the logic path, and the design_margin relates to the sensitivity of the circuit for detecting timing closure.

Flautner teaches the reference signal is delayed with respect to the clock signal by an amount equal to (prop_delay) - (1/2 design_margin), where (prop_delay) is the propagation delay of a processing unit driving the logic path, and the design_margin relates to the sensitivity of the circuit for detecting timing closure [see Flautner: col. 1, line 57-col. 2, line 7].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer and Chuang to include the delay, as taught by Flautner, to compensate additional time and power consumption in recovering the system when a failure occurs [see Flautner: col. 1, line 57-col. 2, line 7].

Response to Arguments

6. Applicant's arguments filed 03/31/2008 have been fully considered but they are not persuasive.

7. Regarding claims 1-4, 6, 10-23, and 27-29 (in which claims 1-3 and 19-21 are currently amended); Applicant argues that Buer does not anticipate the aspect of the present invention [see Applicant's Remarks: Pages 7-9]. Accordingly, Buer discloses claims 1-2, 10-20 and 27-29 (in which claims 1, 2, 19 and 20 are currently amended) [see the above rejections sets forth in this office action].

8. For claims 3-9, and 21-26 (in which, claims 3 and 21 are currently amended), please see the 103(a) rejections sets forth in this office action.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Huynh whose telephone number is 571-272-2718. The examiner can normally be reached on M-F: 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Huynh
Examiner
Art Unit 2857

/Phuong Huynh/
Examiner, Art Unit 2857
July 4, 2008

/Eliseo Ramos-Feliciano/
Supervisory Patent Examiner, Art Unit 2857